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(54) **Non-intrusive microprocessor performance analyzer.**

(57) A set of addresses contained within an address space of an analyzed processor are selected for monitoring according to qualification criteria. Thereafter, address information is placed in a data structure within a control device. Control information from the analyzed processor is monitored and compared against the qualification criteria, and responsive to control information from the analyzed processor agreeing with the qualification criteria, information concurrently present on an address port of the analyzed processor is placed in a temporary storage device. Placement of information in the temporary storage device operates to replace information previously stored therein. A timing device functions to produce indications at regular intervals of time, asychronous with the operation of the analyzed processor. The control device functions, responsive to the indications produced by the timing device, to read the information present in the temporary storage device, compare said information against the set of addresses, and count the number of times the information read from the temporary storage device agrees with information contained within the set of addresses. A count is also maintained of the total number of times information is read from the temporary storage device.

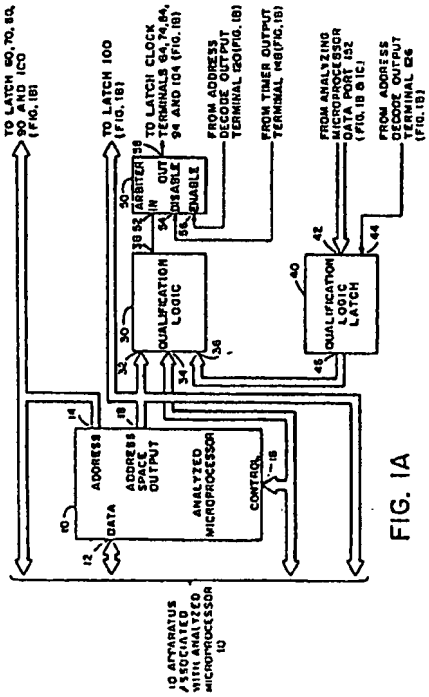

FIG. 1A